Jetson Thor Series Modules

Thermal Design Guide

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Document History

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Version	Date	Description of Change
1.0	June 5, 2025	Initial release
1.1	November 7, 2025	Added Jetson T4000
1.2	March 16, 2026	Updated the following: > Section 3.1.1 thermal performance example
1.3	May 18, 2026	Updated the following: > Updated Figure 3-2: Location of TTP Thermocouple to show module orientation > Added Electrical Design Point definitions

Table of Contents

List of Figures

List of Tables

Chapter 1. Introduction

This document is the thermal design guide (TDG) for the NVIDIA® Jetson T5000™ and Jetson T4000™ modules.

The purpose of this thermal design guide is to provide the system-level thermal, mechanical, and qualification requirements for the Jetson Thor series modules.

1.1 Customer Requirements

The customer requirements are as follows:

- Customers are responsible for reading and understanding this entire thermal design guide.
- Customers are responsible for implementing a thermal solution that maintains the NVIDIA Thor™ system on chip (SoC) and thermal transfer plate (TTP) temperatures below the specified temperatures in Table 2-1 under the maximum thermal load and system conditions for their use case.
- Customers are responsible for designing a system that delivers sufficient power to the Thor Module to sustain the maximum thermal load for their use case.
- Customers are responsible for qualification of the Thor Module in their system and are responsible for any issues related to failure to qualify the product properly.
- The TTP is not designed to be removed by the customer. Removal of the TTP is done solely at the customer's risk.

1.2 Related Documents

The following types of files are associated resources for Thor Module.

- **NVIDIA Jetson Thor Series Module (P3834) 3D CAD STEP model**
  A 3D mechanical model of the board is available in the universal .stp file format. The model is provided to enable system level mechanical fit checks, mounting, and wiring planning.
- **Jetson Thor Series Modules Data Sheet (DS-11955-001)**
  The mechanical drawing of the Thor Module is included in the data sheet.

1.3 Definitions

This section describes terminology that is referenced throughout this thermal design guide.

1.3.1 Total Module Power

The total module power (TMP) represents the average board power dissipation while the system is running the target workload under the worst-case conditions in steady state. System designs must be capable of providing sufficient cooling for the Thor Module when operating at the TMP level.

1.3.1.1 TMP Conditions

TMP conditions for this design are defined under the following operating conditions:

- Worst-case Thor SoC temperature conditions
- Maximum power level for the product configuration
  - The TMP power level is based on the target workload
- Steady state average power

1.3.2 Electrical Design Point

Power rails in the Thor Module can carry high DC currents and are expected to experience large transient current events. The electrical design points (EDP) are specified to guide the power supply design to achieve the desired performance. Due to the dynamic workload seen by the module, the electrical design points are specified within a moving average window.

The aim of power supply design or selection can be categorized into two main areas:

- Sustain continuous average current (EDPc) within target efficiency and thermal performance.
- To achieve a target output voltage overshoot or undershoot specification under a specified large load transient event (EDPp).

The following EDP terms are defined at a product level and not a chip level.

1.3.2.1 EDP Continuous

EDP Continuous (EDPc) is an electrical power (current) requirement defined as the sustained, continuous current drawn by the module. It is typically specified over a long-term moving average timescale of load current while running an intensive application at the target thermal limit. This design point is the highest sustained continuous DC current and serves as the thermal design baseline for the power supply.

Meeting this requirement ensures that the power supply will not shut down during a sustained current draw.

1.3.2.2 EDP Peak

EDP Peak (EDPp) is defined as the maximum peak transient current specified over a short-term moving average timescale. The timescale is shorter than that of EDPc, capturing the brief current transients that occur when the workload transitions from light to heavy operation. Under these conditions, the current can temporarily exceed the EDPc specifications.

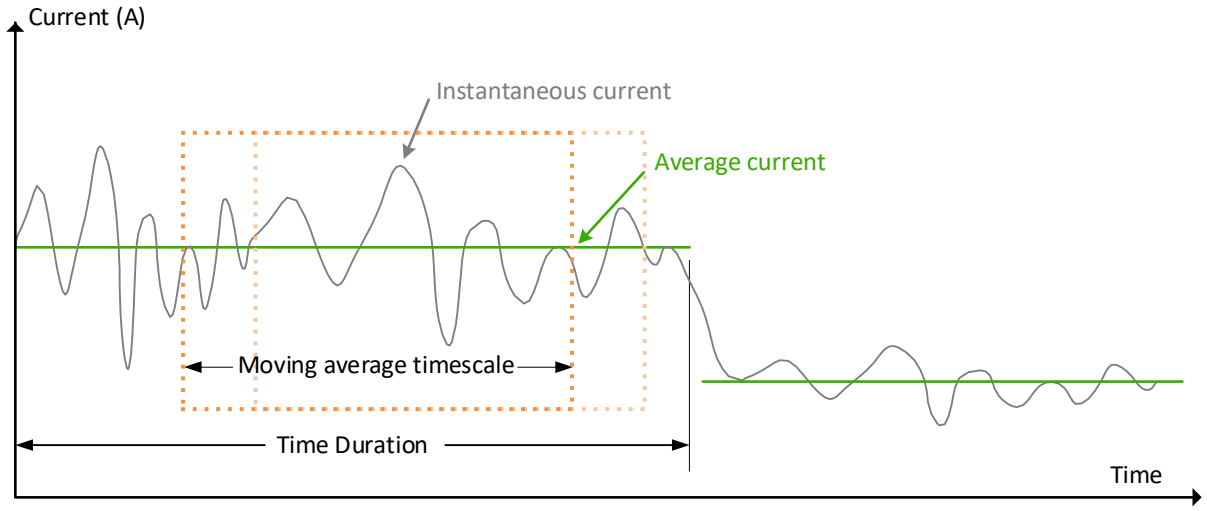
To ensure system stability during these intense bursts, the power supply must tolerate these brief, high-current excursions without triggering over-current protection (OCP) or exceeding the target voltage limits. Properly sizing the power delivery network for these specific transient events prevents unintended system shutdowns during highly dynamic workloads.

The following three parameters specify the Input EDPp:

- Moving average timescale.
- Average current calculated within the timescale.
- Time duration of the average current.

Figure 1-1 illustrates the difference between instantaneous current and moving average current.

Figure 1-1. Input EDPp Moving Average Timescale



Note: EDPp and EDPc are moving average requirements over a specified time window. Instantaneous peak currents exceeding the sustained EDPp and EDPc levels are permissible, provided the moving average within the specified time window is met.

1.3.3 Relationship Between TMP and EDP

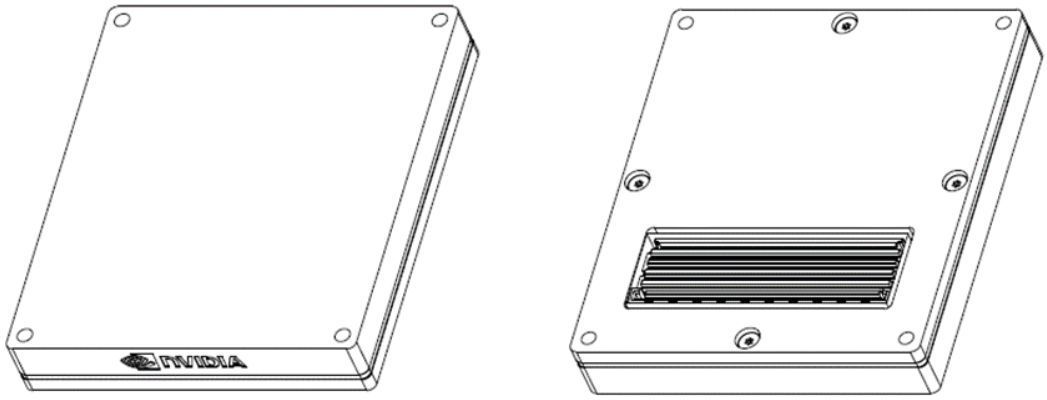
While both metrics relate to power consumption, they address distinct engineering constraints. TMP represents the steady-state average board power dissipation used to size the system-level thermal solution to ensure the Thor SoC and thermal transfer plate (TTP) remains within specified temperature thresholds.

Conversely, EDP values are specified to guide power supply design, ensuring the delivery network can sustain high DC currents and manage large transient events. Specifically, EDPc establishes the sustained electrical design baseline for the power supply. EDPp captures brief, high-current transient excursions caused by changes in workload demand. The power delivery network must tolerate these transients without triggering OCP or causing voltage instability. TMP is the baseline for the system's overall thermal capacity, whereas EDP ensures electrical stability during dynamic operation.

1.3.4 Thermal Transfer Plate

The Thor Module is provided with a thermal transfer plate (TTP) to simplify integration with a system-level thermal solution. The Thor Module is shown in the following figure.

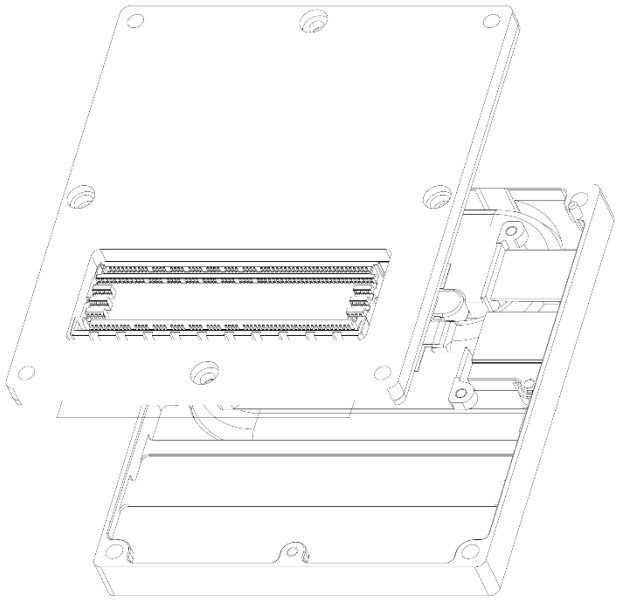
Figure 1-2. Thor Module – 3D View (Top side: Left, Bottom side: Right)



The thermal solution of the customer's system design should attach to the top surface of the TTP with a suitable thermal interface material. The thermal solution can be mounted using the main module mounting holes. More details are provided in Section 3.2.

An exploded view of the Thor Module assembly is shown in Figure 1-3. The PCB is completely covered by the TTP. The TTP design mechanically isolates the PCB and components from external mechanical forces, standardizes the thermal and mechanical interface, and allows for modular system design.

Figure 1-3. Thor Module Design – Exploded View



Note: The warranty becomes void if the TTP is opened.

1.3.5 Thor SoC Temperature

The Thor SoC junction temperature (T_j) represents the Thor SoC die temperature read from the highest of the internal temperature sensors. The on-die thermal sensors are used for high-temperature T_j management and many other temperature-dependent functions. Details regarding the software thermal mechanisms are described in Chapter 4.

Chapter 2. Specifications

2.1 Thermal Specifications

This section provides thermal specifications for Thor Module. On the Thor SoC, there are multiple on-die temperature sensors that are placed close to dominant hotspots to measure temperature and engage thermal protection mechanisms. Chapter 4 contains the details related to these sensors and their thermal protection mechanisms. The specifications in Table 2-1 must be followed to maintain the performance and reliability of the Thor Module.

Table 2-1. Thor Module Thermal Specifications

Parameter	Jetson T5000	Jetson T4000	Units
	MaxN Mode[1]		
Maximum TTP operating temperature[2]	T.TTP = 80.0	T.TTP = 75.0	°C
Recommended Thor SoC operating temperature[3 4 5]	T.SoC = 90.0		°C
Thor SoC maximum operating temperature[5]	T.SoC = 115.0		°C
Thor SoC shutdown temperature[3 4 5]	T.SoC = 118.0		°C

Notes:

1. The MaxN power mode allows for high operating power levels and supports the 130 W for Jetson T5000 or 90 W for Jetson T4000 module power. This thermal offset setting is implemented by NVIDIA to meet product safety and reliability standards and should not be modified.
2. Thermal validation is ongoing. The temperature of the TTP must always be kept within this 80°C for Jetson T5000 or 75°C for Jetson T4000 limit to maintain the specified performance and reliability. The measurement locations are provided in Figure 3-2.
3. The reliability of the Thor Module is set at the recommended Thor SoC Operating temperature limit, 5% of lifetime (5 years) at 118°C and 95% of lifetime at 90°C. Operating above the recommended Thor SoC operating temperature limit will negatively impact the reliability of the Thor SoC and is not recommended. See Section 4.3 for details.
4. The Thor SoC will shut down the Thor Module once this temperature limit is reached to protect the Thor SoC. See Section 4.5 for details.
5. This is the temperature threshold below which the product will operate at the specified clock speeds.

Chapter 3. Design Guidance

This chapter provides design guidance to meet the Thor Module specifications.

3.1 Thermal Information

The design goal for system thermal management is to keep the TTP temperature and the Thor SoC temperature below the limits specified in Section 2.1. The TTP temperature limit maintains the component temperatures on Thor Module within their temperature specifications.

Typical workloads that consume less than 130 W for Jetson T5000 or 90 W for Jetson T4000 module power are likely to operate below the T_j temperature limits, so long as the TTP temperature is within the specification. For unbalanced workloads or higher power workloads, more analysis is needed to evaluate the thermal design. This is described in the following section.

3.1.1 Thor Module Thermal Performance

The Thor Module is designed to have a system level thermal solution attached to the TTP to dissipate the TMP thermal load into the ambient environment. This can be represented with a thermal resistance network where thermal resistance is calculated based on the equation:

$$\theta_{12} = \frac{T_1 - T_2}{P}$$

Where:

θ_{12} The thermal resistance between Point 1 and Point 2

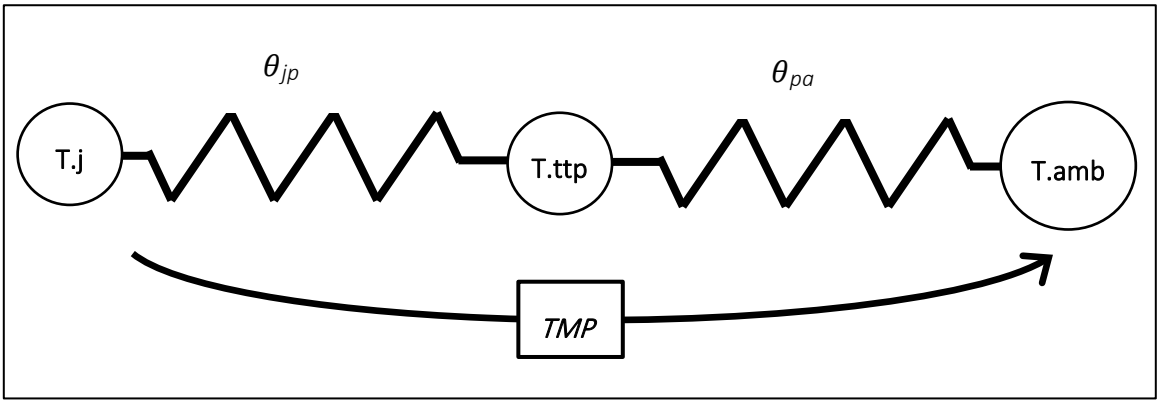
T_n The temperature at Point *n*

P The heat load (for example, dissipated power) transferred between Point 1 and Point 2

A simple example of a thermal resistance network is shown in Figure 3-1, where θ_{jp} represents the thermal resistance from T_j to the TTP and θ_{pa} represents the thermal resistance of the system thermal solution. The thermal resistance of the system thermal

solution may include multiple components including, but not limited to, thermal interface material, heat spreaders, and heat sinks.

Figure 3-1. Thermal Resistance Network



Thor Module enables a wide variety of applications that may exercise different components on the module. The variation between applications will cause variation in heat loads on the different components on the Thor Module and hotspots in different logical partitions of the Thor SoC. While Thor Module is designed to spread the heat and make the thermal performance as consistent as possible, different applications have different levels of thermal performance. The more evenly the module power is distributed across the Thor Module, the better the thermal performance will be. Typical thermal performance of different workloads is listed in the following table.

Table 3-1. Thor Module Thermal Resistance

θ	Jetson T5000		Jetson T40000		Units
	Balanced Workload[1]	Unbalanced Workload[2]	Balanced Workload[1]	Unbalanced Workload[2]	
θ_{jp}	0.180	0.231	0.24	0.30	°C/W
θ_{jb}[3]	6.00		5.3		°C/W

Notes:

1. A balanced workload is well distributed across the CPU, GPU, and DRAM. This is expected to be representative of most use cases.
2. In an unbalanced workload, the power is concentrated on a small area of the Thor SoC. This is not representative of most use cases. An example is a workload that is only running on the CPU partition. Preliminary values subject to change.
3. The θ_{jb} value is provided for simulation of the Thor Module as a 2-resistor model in CFD packages.

The thermal resistance of the module (θ_{jp}) and heat sink (θ_{pa}) sum together for the overall thermal resistance from the Thor SoC to ambient. The required heat sink thermal performance can be determined based on the ambient temperature conditions, use case, and TMP level required by the customer. Consider the following example:

$T.amb = 50°C$

$T.SoC = 90°C$

$\theta jp = 0.18 \frac{°C}{W}$ (Assuming a balanced workload for Jetson T5000)

$P_{TMP} = 60W$

First, check the heat sink thermal performance requirement for the above conditions.

$$\theta_{ja} = \theta_{jp} + \theta_{pa} \rightarrow \theta_{pa} = \theta_{ja} - \theta_{jp} = \frac{90°C - 50°C}{60W} - \theta_{jp} = 0.67\frac{°C}{W} - 0.18\frac{°C}{W} = 0.49\frac{°C}{W}$$

So, the heat sink's thermal performance (θ_{pa}) must be better than 0.49 °C/W. Next, check that the TTP temperature will be below the 80 °C(for Jetson T5000) specification.

$$\theta_{pa} = \frac{T_p - T_a}{P} \rightarrow T_p = \theta_{pa} * P + T_a = 0.49\frac{°C}{W} * 60W + 50°C = 79.4°C$$

So, a 0.49 °C/W or better thermal solution will be sufficient to meet the T_j and TTP temperature specifications.

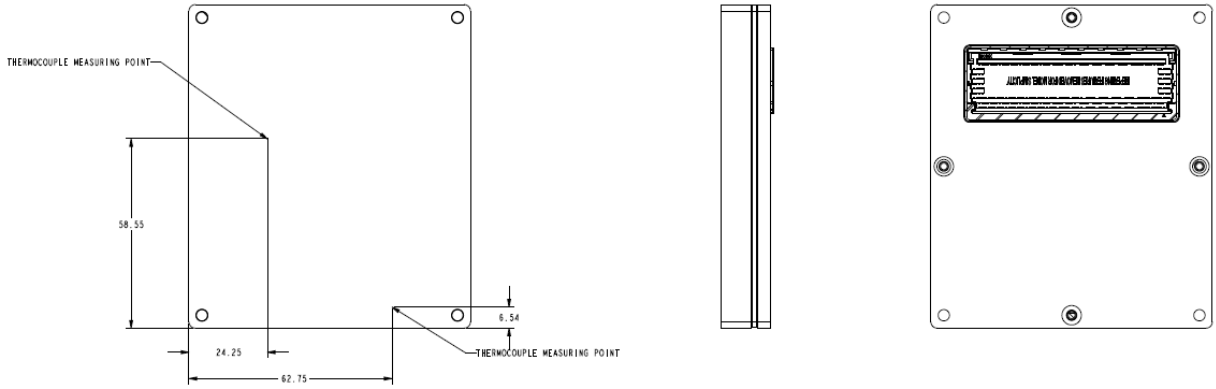
3.1.2 Thor Module Thermal Design Details

The Thor Module product is designed for integration with a product-level thermal solution, which could be a passive heat sink or an active heat sink. The thermal solution must attach to the top surface of the TTP.

The 62.5 × 81.4 mm area, as shown in Figure 3-2, is the key contact area for efficient cooling performance. Full contact with the entire top surface of the TTP is suggested for maximum cooling.

The TTP has a maximum operating temperature specified in Table 2-1. If the Thor Module temperature is kept below this limit, then all other critical components on the PCB will be within their temperature limits as well. The TTP temperature is to be measured during qualification testing at the locations indicated by the "THERMOCOUPLE MEASURING POINT" in Figure 3-2.

Figure 3-2. Location of TTP Thermocouple



In the Z-direction, the cold plate thermocouples should be located on the surface of the TTP, as shown in Figure 3-2. During thermal qualification, these are the only temperatures that need to be monitored with a thermocouple. The Thor SoC temperature will be monitored by the software.

Note the following for Figure 3-3:

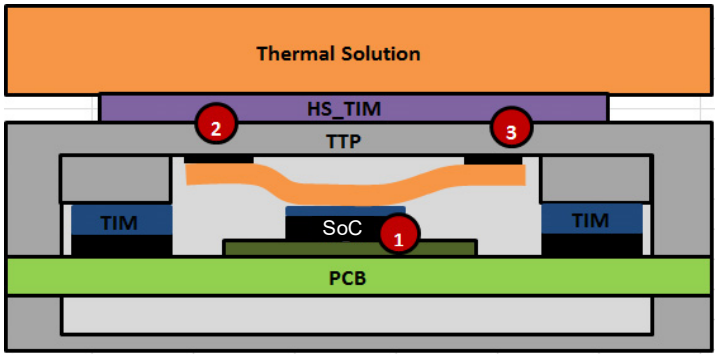
> **Thor Module Contents**

- Thermal transfer plate (TTP) and backside stiffener. The TTP has an internal heat spreader plate connected to the Thor SoC to keep the SoC temperature below its specified temperature limit in Table 2-1.

> **Customer Requirements (The customer is responsible for the following items)**

- HS_TIM. The customer is responsible for providing the thermal interface material (TIM) between the TTP and customer's thermal solution. For best thermal performance, the TIM should provide low thermal impedance within the mechanical, reliability, and cost constraints of the customer's product.
- Thermal Solution. A thermal solution capable of cooling the appropriate amount of TMP for the target workload.
- Maximum TTP Temperature. To ensure that the maximum Thor SoC operating temperature is less than the value specified in Table 2-1 (shown as Location 1 in Figure 3-3), and the maximum TTP temperature must not exceed the value specified in Table 2-1 (shown as Location 2 or 3 in Figure 3-3; the exact location of maximum temperature on TTP will depend on customer use case).

Figure 3-3. Thermal Stack Up Schematic



3.1.3 Customer Thermal Solution

While a variety of customer cooler configurations are possible, the following recommendations should be kept in mind while designing the cooler that interfaces with top of TTP. In all cases however, the following recommendations are applicable:

- Good contact of the thermal solution to the TTP is critical for maximizing the thermal performance of the Thor Module. The Thor SoC is located directly under the TTP and consumes the majority of the TMP. Thus, using a TIM that provides good thermal contact between the thermal solution and the TTP is crucial.
- NVIDIA thermal testing has demonstrated that if the TTP temperature does not exceed the maximum specified temperature, then the rest of the components will be within their specified operating temperature range.
- The customer thermal solution should include adequate margin to account for customer cooler-to-cooler variations.

3.1.4 Temperature Cycling

Long-term reliability of all solder interconnects is negatively impacted by temperature cycling. It is the customer's responsibility to minimize the component's exposure to temperature cycling and to not exceed the limit to which the component is qualified. NVIDIA's Thor SoC is qualified to JEDEC standard JESD47.

Note: NVIDIA recommends that customers refer to JESD94.01 (*Application Specific Qualification Using Knowledge Based Test Methodology*) for more information.

3.2 Mechanical Information

Thor Module partners should refer to the CAD model provided in Section 1.2 for the exact product dimensions to determine how to interface the TTP with their thermal solution and ensure mechanical compatibility in their system. The top view, bottom view, and side views are shown in Figure 3-4, Figure 3-5, and Figure 3-6, respectively.

Figure 3-4. Thor Module Top View

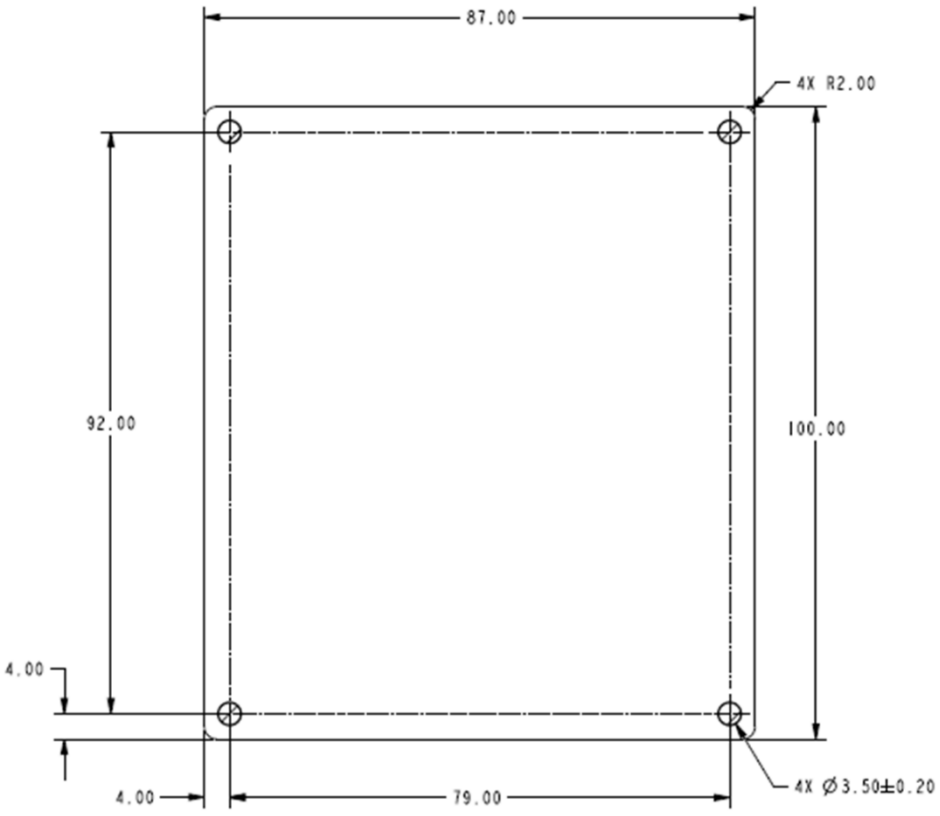


Figure 3-5. Thor Module Bottom View

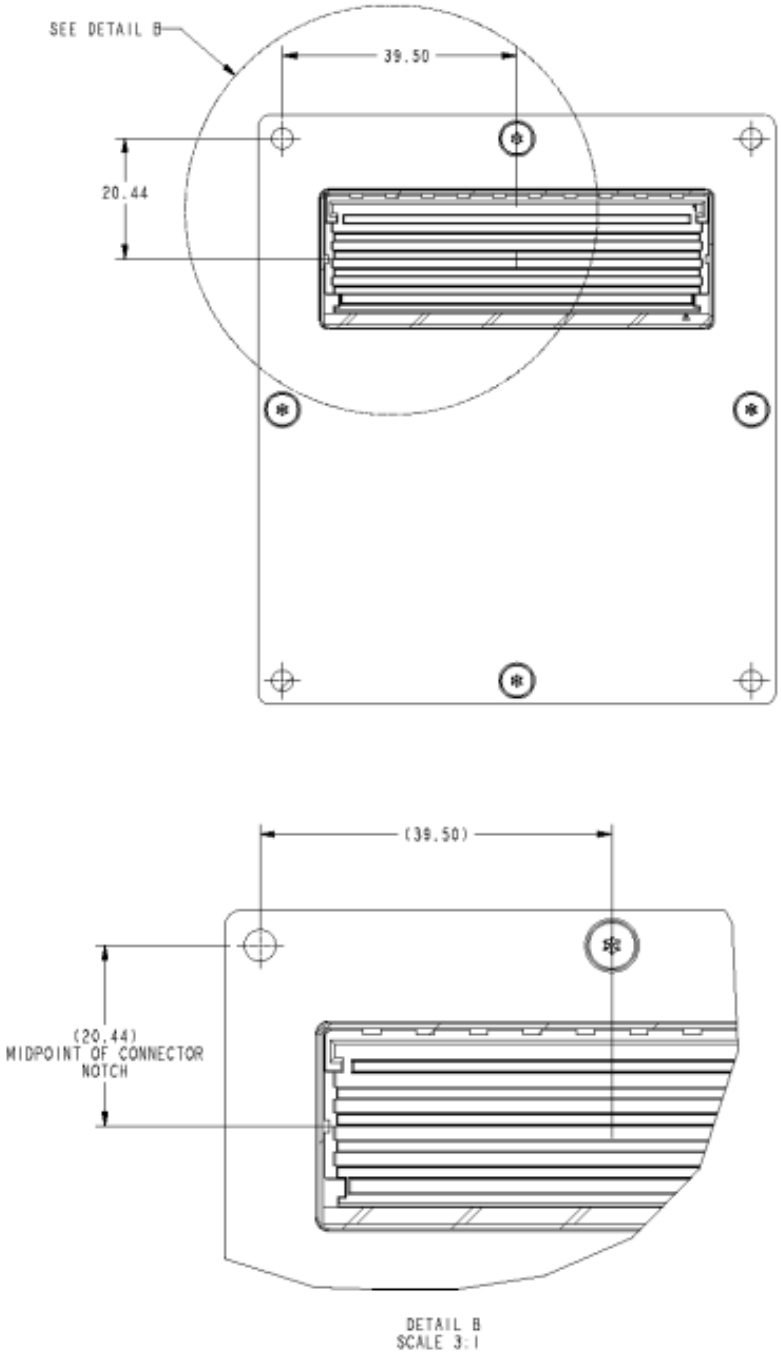
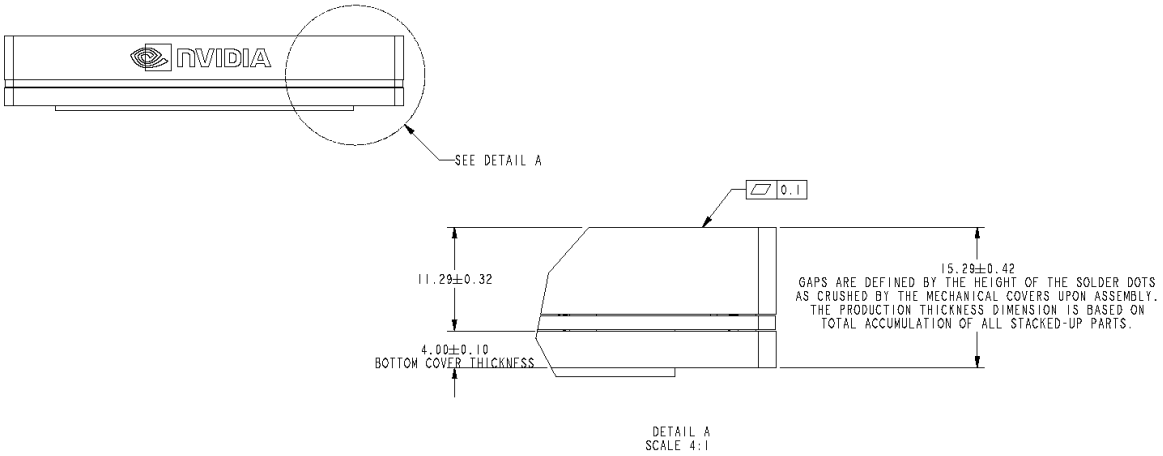


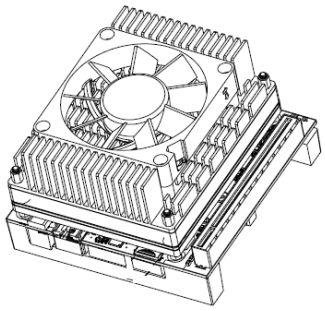
Figure 3-6. Thor Module Side View



3.2.1 Assembly Guidelines

The Thor Module and TTP are provided as a complete unit. Orientation of the unit is to be aligned with the board-to-board connector and secured to the baseboard, as shown in Figure 3-7. Care should be taken to make sure that the mounting screws are not inserted at an angle and that they go through the thermal solution, the TTP, and the backside stiffener. The mounting screws must thread into standoffs that contact the backside stiffener to support the module. Note that the connector alone cannot be used to support the module.

Figure 3-7. Thor Module System Assembly Example

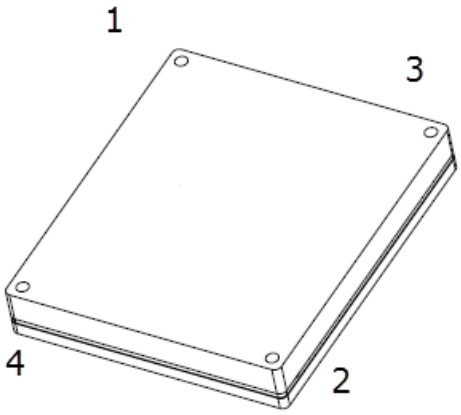


The following are suggested assembly guidelines:

1. Install the Thor Module by carefully aligning the module connector with the base board connector.
2. Insert the module connector into the base board connector.
3. Install each mounting M3 screw into the heat sink.
   a. If the TIM has been pre-applied to the heat sink, make sure to remove the protective cap covering the TIM.

4. Align the heat sink with the module.
5. Each mounting M3 screw should be attached loosely in the sequence shown in Figure 3-8. The tightening sequence should be followed for two cycles. On the last tightening sequence, the screws should be fully torqued.

Figure 3-8. Mounting Screw Sequence



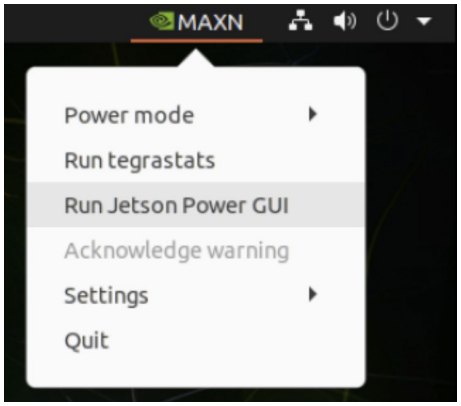
Chapter 4. Software Thermal Management

4.1 Temperature Monitoring

The Jetson Power GUI is a graphical user interface tool for monitoring the power and thermal status of Jetson platforms. The tool reports various power and thermal related information that helps the user to understand power and thermal behavior of Jetson platforms.

To run Jetson Power GUI, follow these two steps:

1. Click the nvpmodel GUI represented by an NVIDIA icon on the right side of the Ubuntu desktop's top bar.
2. Click the "Run Jetson Power GUI" submenu item.



4.2 Fan Control

The Thor Module can be configured to control a system fan. Pulse width modulation (PWM) output and tachometer input are supported. Thor Module has configurable fan control of step-based speed control.

The default fan table is listed in Table 4-1. Note that PWM is configured on a 2^8 scale, with 255 being equivalent to 100% duty cycle.

Table 4-1. Thor Module Default Fan

Tmargin[2] (°C)	PWM	Fan RPM
1	255	2900
9	255	2900
10	215	2440
28	215	2440
58	66	750
112	66	750

Notes:

1. This table is an example, and fan control architecture is subject to change with the next software release. Customers must verify their own thermal solution with real software in the expected environment.
2. TMARGIN temperature is defined in software code. Refer to the *Jetson Linux Developer Guide*.

4.3 Thor SoC Recommended Operating Temperature Limit

The recommended operating temperature limit is the threshold at which the module will operate without performance reduction. These temperatures are listed in Table 2-1 and cannot be adjusted. The customer's tolerance for performance reduction should determine the amount of T_j operating headroom in the thermal solution design to accommodate the temperature sensor uncertainty of ±3 °C.

Software thermal management operates as follows:

- When the measured temperature is at or below the operating temperature threshold, software T_j thermal management is not engaged. The system is free to vary the system frequencies and voltages by the DVFS algorithm.
- When the measured temperature reaches the thermal management threshold, the internal thermal sensors generate an interrupt to software. At this point, the software thermal management algorithm engages and begins periodically performing the following operations:
  - Polling temperature
  - Running a thermal management control algorithm to calculate the throttle degree, indicating the amount of throttling to apply during the next time period.
  - Throttle the system to the level of throttling indicated by the throttling control algorithm. Throttling is applied through limits on the clock frequency of high-power units such as the CPU and GPU. Higher throttling degree results in lower frequency limits. DVFS policies operate within these frequency limits.
- Software thermal management remains in operation until the Thor SoC temperature has returned to a value below the throttling threshold and throttling degree has returned to zero.

Note:

1. Power fluctuations that induce T_j fluctuations above the software thermal management thresholds will cause temporary clock reductions. Power fluctuations in the target workload should be evaluated for their potential to cause temperature to fluctuate above the software threshold.
2. Refer to the *Jetson Linux Developer Guide* for thermal management in software.

4.4 Thor SoC Hardware Thermal Throttling

If the software thermal management is not able to maintain the Thor SoC temperature, then the hardware thermal throttling will attempt to prevent an over-temperature thermal trip. Thermal trips on Jetson Thor cause the system to reset. To avoid thermal trip conditions without being overly conservative, Thor SoC has hardware-engaged clock throttling mechanisms that are used as a last resort to prevent thermal trip conditions. This will lower the Thor SoC temperature, but it will also significantly reduce the overall Thor SoC performance. The Thor SoC throttle settings cannot be altered. These settings are implemented by NVIDIA to meet product safety and reliability standards.

4.5 Thor SoC Thermal Trip Temperature

The Thor SoC is rated to operate at a junction temperature not to exceed 118 °C. Thor Module has hardware thermal trip mechanisms that enforce this limit by automatically performing a system reset when this temperature is exceeded.

The thermal trip temperature should not be reached at any time during normal operation, but it may occur if cooling system components are broken, jammed, or otherwise unable to cool the Thor SoC under worst-case conditions. If a thermal trip event is triggered, then a major fault in the Thor Module or system cooling solution has occurred. Thermal trip can be initiated by any of the sensors listed in Table 2-1. Using multiple sensors enables operation closer to the temperature limit without compromising reliability by reducing the uncertainty associated with the hotspot location.

The following thermal trip mechanisms have been Implemented:

- Internal sensor-based thermal trip. Failsafe thermal trip is guaranteed by using the thermal trip signal directly from the SoC to the PMIC. After the failsafe thermal trip, the system will reset without the user pressing the power button or equivalent input.
- T.diode and temperature-monitor-based thermal trip. When the external temperature monitor detects that the T.diode temperature is above a pre-programmed thermal trip, the monitor's THERM output signals the PMIC to reset the system without any software control. This is a backup mechanism to the internal

sensor-based thermal trip, so it is intentionally margined to a higher temperature to avoid contention with internal sensor-based thermal trip.

The Thor SoC thermal trip settings cannot be altered. These settings are implemented by NVIDIA to meet product safety and reliability standards.

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